

FIG. 1 is a schematic cross-sectional view of a semiconductor device 100. The device includes a central core 10 with a vertical channel 4. The core is surrounded by a layer 13. The entire structure is enclosed in a frame 30. The top and bottom surfaces are labeled DO and LO, respectively. The side walls are labeled B. The central channel 4 is filled with a material having a different texture than the surrounding layers. Dimensions X and Y are indicated.

FIG.2

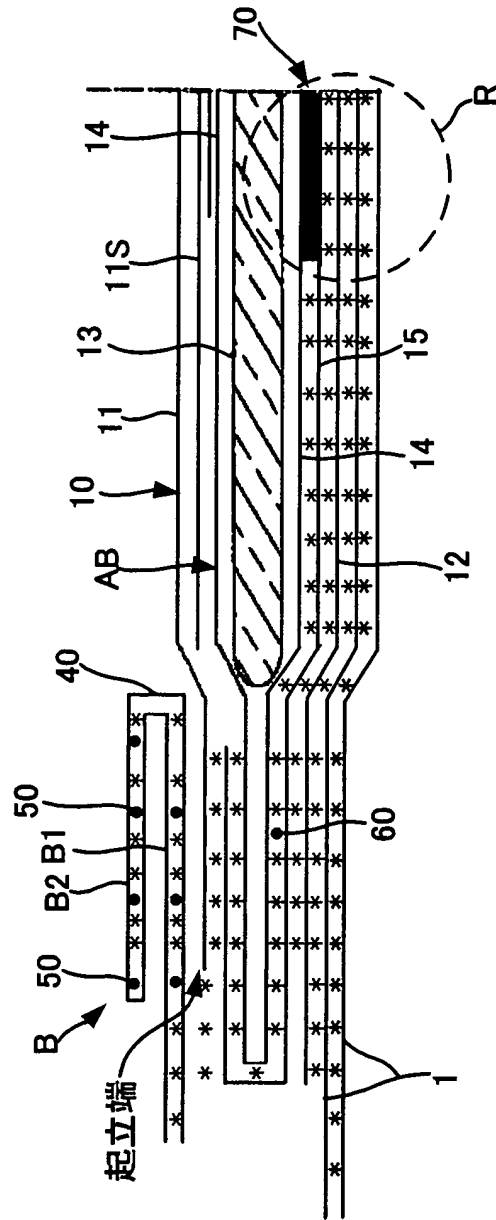




FIG.4

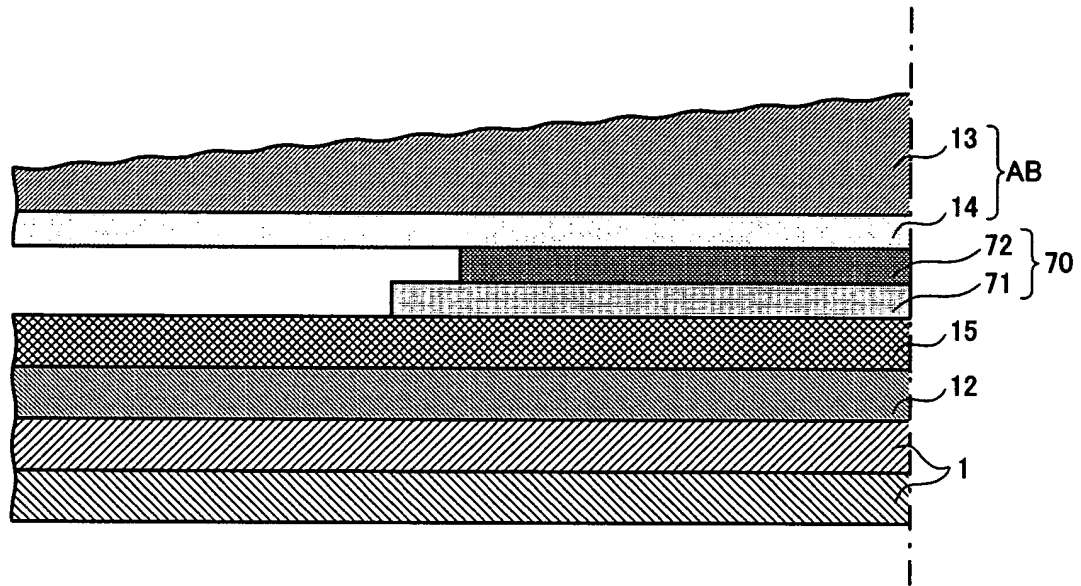


FIG.5

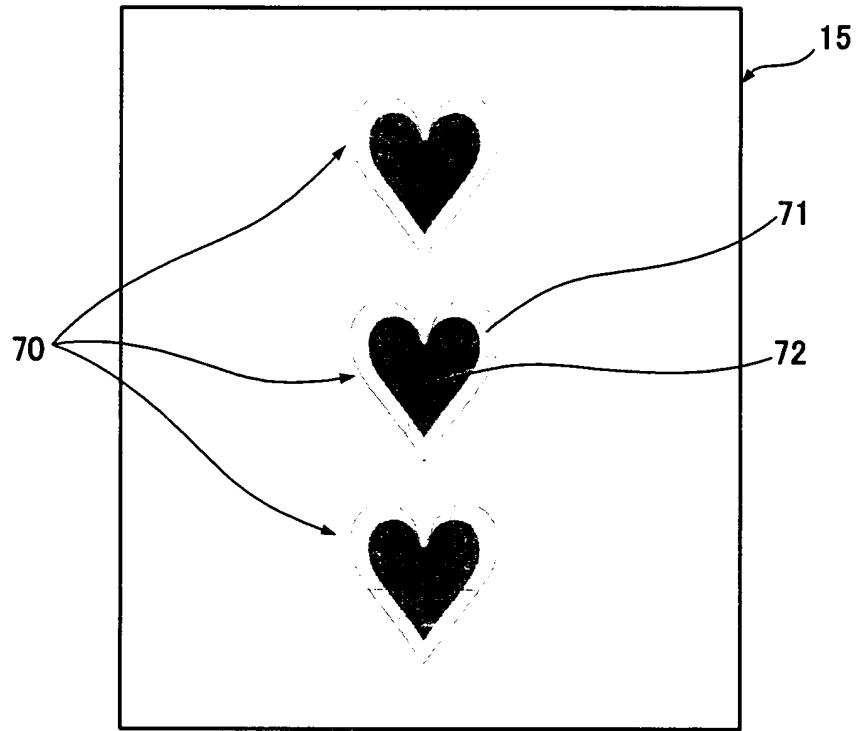


FIG.6

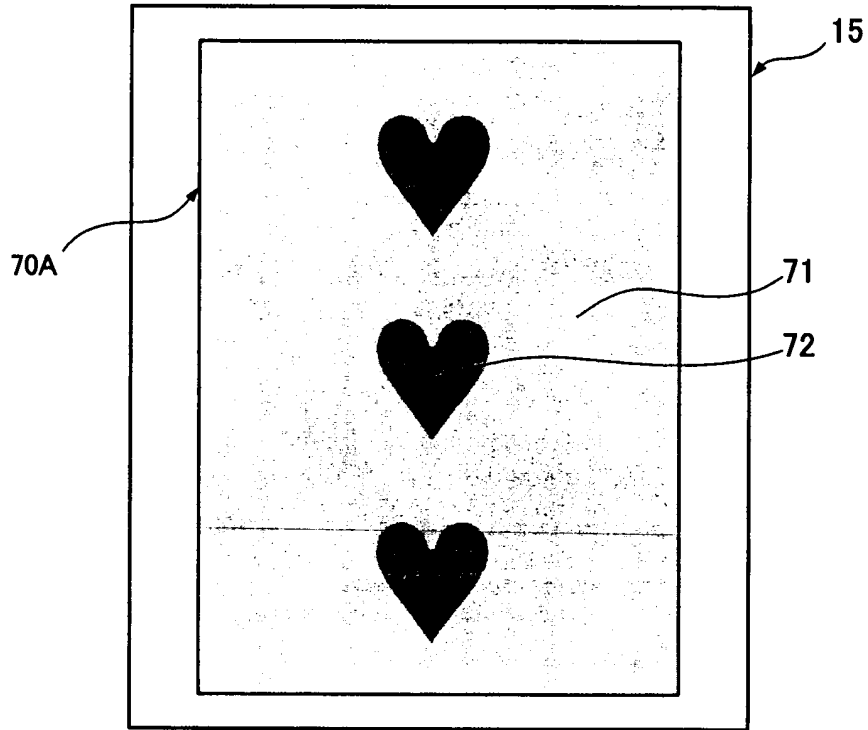


FIG.7

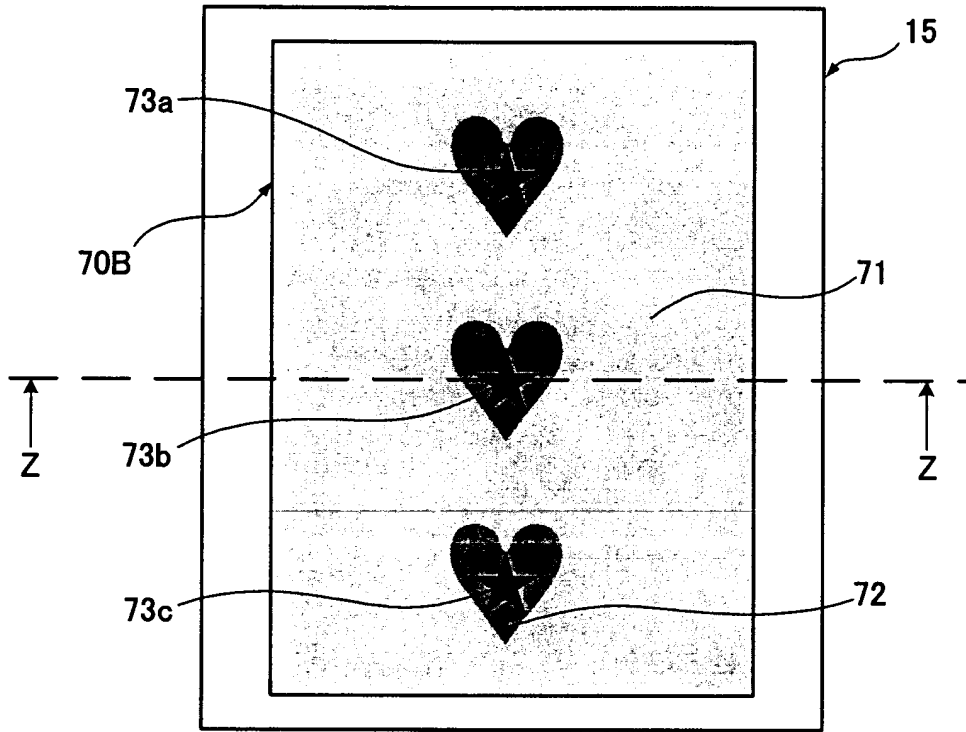


FIG.8

